REMARKS

With this amendment Claims 8-23 and 25-28 are pending in the present application, and Claims 15 and 21 have been amended. The specific changes to the amended claims are shown on a separate set of pages attached hereto and entitled VERSION WITH MARKINGS TO SHOW CHANGES MADE, which follows the signature page of this Amendment. On this set of pages, the insertions are underlined while the ~~deletions are stricken through~~. In view of the foregoing amendments and the following remarks, Applicant respectfully requests reconsideration and allowance of this application.

Objections to the Drawings

The Examiner objected to the drawings, asserting that the Figures are improperly crosshatched. Appropriate corrections have been made and are attached on a separate set of pages following the page entitled Proposed Drawing Changes.

Definiteness Under 35 U.S.C. § 112

Claims 21-23 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In particular, the Examiner asserted that Claim 21 was rejected as being incomplete for omitting essential structural cooperative relationships of elements. Specifically, the Examiner asserts that the location of the flexible tape relative to the die and the die attach layer is omitted.

Claims 21 has been amended as indicated above to include a recitation of the location of the flexible tape relative to the die and the die attach layer. Thus Applicant respectfully requests that these rejections be withdrawn.

Non-Obviousness under 35 U.S.C. § 103

Claims 8-23 and 25-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over the publication "Tessera's Micro Ball Grid Array, Chapter 16" (hereafter referred to as "Tessera").

Claims 8-14 Are Not Obvious

Regarding Claim 8, the Examiner asserts that Tessera teaches an integrated circuit package (FIGURE 16.2), comprising: a die; a die attach layer (labeled as elastomeric compliant layer) over the die; and an array of solder balls over the die attach layer. The Examiner further asserts that Tessera fails to explicitly teach that the die attach layer has a

coefficient of thermal expansion of less than about 106 ppm/°C. The Examiner asserts that Tessera teaches that "it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, line 2 – p. 265 line 2." The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 106 ppm/°C.

Applicant traverses the rejection and respectfully disagrees with the Examiner's characterization of the cited reference. Tessera does not teach or suggest, explicitly, implicitly, or inherently, providing a die attach layer having the properties recited in Applicant's Claim 8. Applicant submits that one skilled in the art would not have known to use a die attach layer having a coefficient of thermal expansion of less than about 106 ppm/°C in an integrated circuit package as recited in Applicant's Claim 8, because the importance of this property of the die attach layer was not recognized by Tessera. Moreover, Applicant submits that that the Examiner has not pointed to any reference which indicates that a die attach layer having the properties recited in Claim 8 was known to those skilled in the art.

Applicant respectfully submits that Tessera does not teach a die attach layer with a thermal expansion coefficient as close as possible to the chip and to the substrate. The purpose of the compliant layer taught by Tessera is to relieve the stresses due to the thermal mismatch between the silicon chip and the substrate by providing a flexible, compliant elastomer with a very low Young's modulus (0.0061 Gpa equal to about 0.885 ksi according to Table 16.12 on page 276 of Tessera). The compliant layer is expected to flex as the chip and substrate expand and contract relative to one another. Compliant leads are provided in order to allow a flexible electronic connection between the chip and the substrate.

Applicant respectfully submits that Tessera clearly does not consider the Coefficient of Thermal Expansion (CTE) of the elastomer layer itself to be an important property. Page 264, lines 9-10 of Tessera state, "In general, a thicker elastomer yields a higher effective CTE, but lower package stiffness." Thus, the elastomer layer taught by Tessera has a

substantially higher thermal expansion coefficient than the other package components. This is clearly shown in Table 16.12 on page 276 of Tessera. Table 16.12 lists the "elastomer" as having a thermal expansion coefficient of 200 ppm/°C. The elastomer layer of Tessera relieves stresses between the chip and the substrate merely by being compliant and allowing the chip and substrate to freely expand and contract relative to one another. Thus Tessera clearly does not teach, either explicitly or implicitly, using an adhesive with a CTE of less than about 106 ppm/°C, and in fact Tessera teaches away from using an elastomer layer having a low thermal expansion coefficient by teaching an elastomer with a much higher CTE. For at least these reasons, Applicant respectfully submits that it would not have been obvious to one of skill in the art at the time the invention was made to provide an integrated circuit package as recited in Claim 8. Thus, Applicant respectfully requests that the rejection of Claim 8 be withdrawn.

Claims 9-14 depend from Claim 8, and include the unique combination of limitations of the base claim as well as additional unique combinations of features also not taught or suggested by the prior art of record. Thus Applicant respectfully requests that the rejections of Claims 9-14 also be withdrawn.

Claims 15 and 16 Are Not Obvious

Regarding Claim 15, the Examiner asserts that Tessera teaches an integrated circuit package (FIGURE 16.2), comprising: a die; a die attach layer (labeled as elastomeric compliant layer) over the die; and an array of solder balls over the die attach layer. The Examiner asserts that in addition, Tessera teaches that the die attach layer is an elastomeric compliant layer, and that it is therefore inherent that the die attach layer has a modulus of elasticity of less than about 126 ksi. The Examiner further asserts that Tessera fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C. The Examiner asserts that Tessera teaches that "it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, line 2 – p. 265 line 2." The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a die attach layer

having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 106 ppm/°C.

Applicant traverses the rejection and respectfully submits that the Examiner has not established a *prima facie* case of obviousness. Applicant respectfully submits that nowhere does Tessera teach or suggest a die attach layer having the unique combination of properties recited in Applicant's Claim 15. Applicant submits that one skilled in the art would not have known to use a die attach layer having a coefficient of thermal expansion of less than about 106 ppm/°C and a modulus of elasticity of less than about 126 ksi and greater than about 10 ksi in an integrated circuit package as recited in Applicant's Claim 15, because the importance of these properties of the die attach layer was not recognized by Tessera. Moreover, Applicant submits that that the Examiner has not pointed to any reference which indicates that a die attach layer having the properties recited in Claim 15 was known to those skilled in the art.

Tessera actually teaches relieving stresses between the chip and the substrate by using an elastomer layer with a high CTE (200 ppm/°C) and a "low" modulus of elasticity (0.0061 Gpa equal to about 0.885 ksi according to Table 16.12 on page 276 of Tessera). The elastomer layer of Tessera relieves stresses between the chip and the substrate merely by being compliant and allowing the chip and substrate to freely expand and contract relative to one another. Tessera does not recognize the importance of the compliant layer having a relatively low coefficient of thermal expansion and a modulus of elasticity which is neither too low nor too high.

As described in the specification of the above-identified application, at page 2, line 22 through page 3, line 5, the prior art has generally used die attach layers having a low modulus of elasticity, and a high coefficient of thermal expansion. Because of the die attach layer's high coefficient of thermal expansion and compliance relative to the die, the die attach layer expands and shrinks more rapidly than the die during thermal exposure. This creates stress on the conductive leads connecting the solder ball array to the die, and causes breakage of the leads from the die. By recognizing the relationship between these properties of the die attach layer as compared to those of a typical die, and by providing an integrated circuit package using a die attach layer with substantially different properties from those of die attach layers

of the prior art, Applicant in one embodiment has provided an integrated circuit package with a substantially reduced tendency to suffer from the problem known as heel break.

Applicant respectfully submits that Tessera does not suggest providing a die attach layer with the properties recited in Applicant's Claim 15 in order to address the problem of heel break. In fact, by teaching the use of an elastomer with a CTE which is substantially higher than that recited in Claim 15, and a modulus of elasticity which is substantially below the range recited in Claim 15, Tessera teaches away from the die attach layer recited in Claim 15. Furthermore, the Examiner has not provided any reference indicating that a die attach layer having the properties recited in Claim 15 was known. Applicant therefore respectfully submits that providing a die attach layer having a coefficient of thermal expansion of less than about 106 ppm/°C and a modulus of elasticity of less than about 126 ksi and greater than about 10 ksi as recited in Claim 15 would not have been obvious to one of skill in the art at the time the invention was made. Thus, Applicant respectfully requests that the rejection of Claim 15 be withdrawn.

Claim 16 depends from Claim 15, and includes the unique combinations of limitations of the base claim as well as additional unique combinations of features also not taught or suggested by the prior art of record. Thus Applicant respectfully requests that the rejection of Claim 16 also be withdrawn.

Claims 17-20 Are Not Obvious

Regarding Claim 17, the Examiner asserts that Tessera teaches an integrated circuit package (FIGURE 16.2), comprising: a die; a die attach layer (labeled as elastomeric compliant layer) over the die; and an array of solder balls over the die attach layer. The Examiner further asserts that Tessera fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 200 ppm/°C. The Examiner asserts that Tessera teaches that "it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, line 2 – p. 265 line 2." The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient as

close as possible to the chip and to the substrate which would inherently be less than about 200 ppm/°C.

Applicant traverses the rejection and respectfully disagrees with the Examiner's characterization of the cited reference. Applicant respectfully submits that nowhere does Tessera teach or suggest a die attach layer having the unique combination of properties recited in Applicant's Claim 17. As discussed above, Tessera does not teach a die attach layer with a thermal expansion coefficient as close as possible to the chip and to the substrate. In fact as discussed above, Tessera teaches a high CTE (for example, 200 ppm/°C). Therefore, Tessera does not teach, either explicitly or implicitly, that the CTE should be less than about 200 ppm/°C. Thus, Applicant respectfully requests that the rejection of Claim 17 be withdrawn.

Claims 18-20 depend from Claim 17, and include the unique combinations of limitations of the base claim as well as additional unique combinations of features also not taught or suggested by the prior art of record. Thus Applicant respectfully requests that the rejection of Claims 18-20 also be withdrawn.

Claims 21-23 Are Not Obvious

Regarding Claim 21, the Examiner asserts that Tessera teaches an integrated circuit package (FIGURE 16.2), comprising: a die; a die attach layer (labeled as elastomeric compliant layer) over the die; and an array of solder balls over the die attach layer. The Examiner asserts that in addition, Tessera teaches that the die attach layer is an elastomeric compliant layer, and that it is therefore inherent that the die attach layer has a modulus of elasticity of less than about 126 ksi. The Examiner further asserts that Tessera fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 200 ppm/°C. The Examiner asserts that Tessera teaches that "it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, line 2 – p. 265 line 2." The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a die attach layer having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 200 ppm/°C. The Examiner further asserts that it

has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Applicant respectfully traverses the rejection and the Examiner's characterization of the cited art. For substantially the same reasons given above with respect to Claims 8 and 15, Applicant respectfully submits that Tessera does not teach or suggest a die attach layer having the properties recited in Claim 21.

Moreover, Applicant respectfully disagrees with the characterization of these limitations as being simply "optimum" ranges. Applicant submits that a rejection based on "optimum or workable ranges" is inappropriate where the prior art does not teach or suggest the desirability of the result achieved. As discussed in MPEP § 2144.05, "[a] particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation." In re Antonie, 559 F.2d 618, 195 U.S.P.Q. 6 (CCPA 1977). Thus, for a rejection to be made based on "optimum or workable ranges," the prior art must first identify the result which the variable achieves.

As discussed above, in one embodiment of the above-identified application, the problem of thermally induced heel break can be substantially eliminated by providing a die attach layer with a coefficient of thermal expansion less than about 200 ppm/°C and a modulus of elasticity of between about 10 ksi and about 126 ksi. As described at page 9, lines 23-29 of the specification of the present application, a higher modulus of elasticity will decrease the movement within the compliant layer, and will thereby decrease the stress at the heel. Thus, by providing a compliant layer with a modulus of elasticity which is higher than has been used in the prior art, the problem of heel break can be substantially avoided.

Applicant respectfully submits that nowhere does Tessera teach or suggest the desirability of varying either the coefficient of thermal expansion or the modulus of elasticity in addressing the problem of heel breakage. Accordingly, without disclosing this desired result, Tessera cannot be used to reject the claims on the basis that the parameters affecting this result are merely "optimum or workable" ranges that would be known to one of skill in the art. Moreover, the modulus of elasticity taught by Tessera (0.0061 GPa equal to about 0.885 ksi) is so much smaller than the ranges taught by certain of Applicant's embodiments,

that Tessera actually teaches away from the ranges recited in Applicant's Claims 21-23. Thus, Applicant respectfully requests that the rejection of Claim 21 be withdrawn.

Claims 22 and 23 depend from Claim 21, and include the unique combinations of limitations of the base claim as well as additional unique combinations of features also not taught or suggested by the prior art of record. Thus Applicant respectfully requests that the rejection of Claims 22 and 23 also be withdrawn.

Claims 25-28 Are Not Obvious

Claims 25-28 were rejected under 35 U.S.C. § 103(a) for substantially the same reasons discussed above. As discussed above, Applicant respectfully traverses the rejection and requests reconsideration.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant submits that this application, as amended, is in condition for allowance and such action is respectfully requested. The undersigned has made a good faith effort to respond to all of the rejections and objections in the case, and to place the claims in condition for immediate allowance. Nevertheless, if any undeveloped issues remain or if any issues require clarification, the Examiner is respectfully requested to call Applicant's counsel at the number indicated below in order to resolve such issues promptly.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 1/23/03

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VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE CLAIMS

Claims 15 and 21 have been amended as follows:

15. **(AMENDED)** An integrated circuit package, comprising:

a die;

a die attach layer over the die; and

an array of solder balls over the die attach layer;

wherein the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C and a modulus of elasticity of less than about 126 ksi and greater than about 10 ksi.

21. **(AMENDED)** A first level integrated circuit package, comprising:

a first level package including a chip;

an array of solder balls for connecting the first level package to a second level package;

an adhesive layer between the chip and the array of solder balls, the adhesive layer having a coefficient of thermal expansion of less than about 200 ppm/°C; and

a flexible tape connecting the array to the chip, wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip;

wherein the adhesive layer has a modulus of elasticity of greater than about 10 ksi and less than about 126 ksi.